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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,109	12/07/2004	Martin Wagner	DE 020140	1318

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EXAMINER	
SCHELL, JOSEPH O	

ART UNIT	PAPER NUMBER
2114	

NOTIFICATION DATE	DELIVERY MODE
06/02/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/517,109	WAGNER ET AL.	
	Examiner	Art Unit	
	JOSEPH SCHELL	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 1-9 and 11-16 have been examined.

Claims 1-9 and 11-16 have been rejected.

Response to Arguments

The remarks submitted April 1, 2009 have been fully considered but any arguments therein are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 5 and 9-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Carter (US Patent 6,298,449).

As per claim 1, Carter ('449) discloses a method of monitoring the operation of at least one microcontroller unit that is associated with a system, the method comprising:

associating at least one non-volatile memory area with the microcontroller unit

(the error log memory 28 of Figure 2, preferably non-volatile as stated in column 5 lines 16-20), wherein the memory area can be read from and written to by the microcontroller unit (column 4 lines 35-42 and column 8 lines 32-35, the log is accessible for diagnostic purposes); and

storing at least one set of statistics relating to the operation of the microcontroller unit, including at least a set of fault statistics for the microcontroller, by means of the non-volatile memory area (column 2 lines 31-34).

As per claim 2, Carter ('449) discloses a method as claimed in claim 1, wherein the memory area is permanently supplied by at least one battery unit (column 7 lines 23-25, an uninterruptible power supply uses a battery).

As per claim 5, Carter ('449) discloses a base chip for monitoring the operation of at least one microcontroller unit, including at least one non-volatile memory area (column 5 lines 16-20) that can be read from and written to by the microcontroller unit (column 4 lines 35-42 and column 8 lines 32-35), and by means of which at least one set of fault statistics relating to operation of the microcontroller unit, can be produced (column 2 lines 36-40, a record of events is created).

As per claim 9-5, Carter ('449) discloses a system including at least one microcontroller unit intended for at least one application and at least one base chip as claimed in claim 5 (the system as shown in Figure 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 6, 7, 8, 9-6, 9-7, 11, 12, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carter ('449) in view of Daudelin ('532) (from the PTO-892 filed December 1, 2008).

As per claim 3, Carter ('449) discloses a method as claimed in claim 1 or 2. carter ('449) does not expressly disclose the method wherein in relation to the operation of the microcontroller unit a distinction can be made between different reset events, and these different reset events can be made accessible to the microcontroller unit.

Daudelin ('532) teaches a system that counts software reset events, compares the count to a threshold, and switches to a known good software when the threshold is reached (abstract and Figure 4).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the platform reliability system disclosed by Carter ('449) such that, in addition to power failure events being logged (column 2 lines 47-53), software reset events are

additionally counted for comparison to a threshold, as taught by Daudelin ('532). This modification would have been obvious because it allows determine that software is nonfunctional and to take additional repair steps (Daudelin ('532) column 2 lines 32-44).

As per claim 6, Carter ('449) discloses a base chip as claimed in claim 5, including at least one reset unit for resetting the microcontroller unit, which reset unit is connected to the microcontroller unit (column 2 lines 4-7, the remote rebooting unit), and at least one supply unit that is connected to the microcontroller unit (as shown in Figure 2, the reliability card 10 may be considered a supply unit because it receives alarm signals from the power supply 16).

Carter ('449) does not expressly disclose the base chip including at least one information unit that is provided to allow for different reset events.

Daudelin ('532) teaches a system that counts software reset events, compares the count to a threshold, and switches to a known good software when the threshold is reached (abstract and Figure 4).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the platform reliability system disclosed by Carter ('449) such that, in addition to power failure events being logged (column 2 lines 47-53), software reset events are additionally counted for comparison to a threshold, as taught by Daudelin ('532). This

modification would have been obvious because it allows determine that software is nonfunctional and to take additional repair steps (Daudelin ('532) column 2 lines 32-44).

As per claim 7, Carter ('449) in view of Daudelin ('532) discloses a base chip as claimed in claim 6, wherein the memory area and the supply unit are permanently supplied with power from at least one battery unit (Carter ('449) column 7 lines 23-25, an uninterruptible power supply uses a battery), and the microcontroller unit has at least one temporary energy supply provided to it via the supply unit (Carter ('449) column 2 lines 5-8, the power supply controller provides the primary or secondary power).

As per claim 8, Carter ('449) in view of Daudelin ('532) discloses a base chip as claimed in any of claims 6 to 7, wherein the memory area and the information unit have inserted in front of them at least one interface unit for exchange of data with the microcontroller unit (Carter ('449) Figure 3 shows a bus between the processor 60 and memory area 44 and a bus between the processor 60 and the power supply controller 54).

As per claims 9-6 and 9-7, Carter ('449) in view of Daudelin ('532) discloses a system including at least one microcontroller unit intended for at least one application and at least one base chip as claimed in any of claims 6 to 7 (Carter ('449) the system as shown in Figure 2).

As per claim 11, Carter ('449) discloses the method of claim 1. Carter ('449) does not expressly disclose the method wherein the fault statistics include statistics on a plurality of different types of reset events.

Daudelin ('532) teaches a system that counts software reset events, compares the count to a threshold, and switches to a known good software when the threshold is reached (abstract and Figure 4).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the platform reliability system disclosed by Carter ('449) such that, in addition to power failure events being logged (column 2 lines 47-53), software reset events are additionally counted for comparison to a threshold, as taught by Daudelin ('532). This modification would have been obvious because it allows determine that software is nonfunctional and to take additional repair steps (Daudelin ('532) column 2 lines 32-44).

As per claim 12, Carter ('449) in view of Daudelin ('532) discloses the method of claim 11, further comprising:

comparing a number of at least one type of reset event to a threshold (Daudelin ('532) column 2 lines 37-42); and

when the number of the at least one type of reset event is greater than the threshold, operating the microcontroller unit in a low-energy mode (Carter ('449) column 7 lines 23-32 describe a UPS available during power failures. At the time of invention it

would have been obvious to a person of ordinary skill in the art that, during a power failure as described by Carter ('449), a software reset threshold causes a low power mode to be enacted by the controller instead of immediately performing a software upgrade (as is shown in Daudelin ('532) Figure 4) for reasons of power conservation by the monitoring system).

As per claims 14 and 15, these claims recite limitations found in claims 11 and 12, respectively, and are respectively rejected on the same grounds as claim 11 and 12.

Claims 4 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carter ('449) in view of Jablon ('006) (from the PTO-892 filed October 3, 2006).

As per claim 4, Carter ('449) discloses the method as claimed in any of claims 1 to 2. Carter ('449) does not expressly disclose the method further comprising permitting the non-volatile memory area to be read from at any time; and permitting the non-volatile memory area to be written only while the system is starting.

Jablon ('006) teaches a write protection scheme wherein a memory is locked as read only except during a boot up (column 8 lines 20-33).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the monitoring system disclosed by Carter ('449) such that it employs a write

protected memory scheme as taught by Jablon ('006). This modification would have been obvious because it prevents software attacks on stored data (Jablon ('006) column 8 lines 34-38).

As per claim 16, this claim recites limitations found in claim 4 and is rejected on the same grounds as claim 4.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Carter ('449) in view of NAND vs. NOR Flash Technology by Arie Tal (herein Tal).

Carter ('449) discloses the base chip of claim 5. Carter ('449) does not expressly disclose the base chip wherein the at least one non-volatile memory area comprises a random access memory.

Tal teaches features of NAND and NOR type flash memories.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the non-volatile memory disclosed in the system of Tal such that it is a flash memory. This modification would have been obvious because NOR flash memory delivers a high read performance and is cost effective is low capacities (Tal, fourth paragraph).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH SCHELL whose telephone number is (571)272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Scott T Baderman/
Supervisory Patent Examiner, Art Unit 2114

JS